100

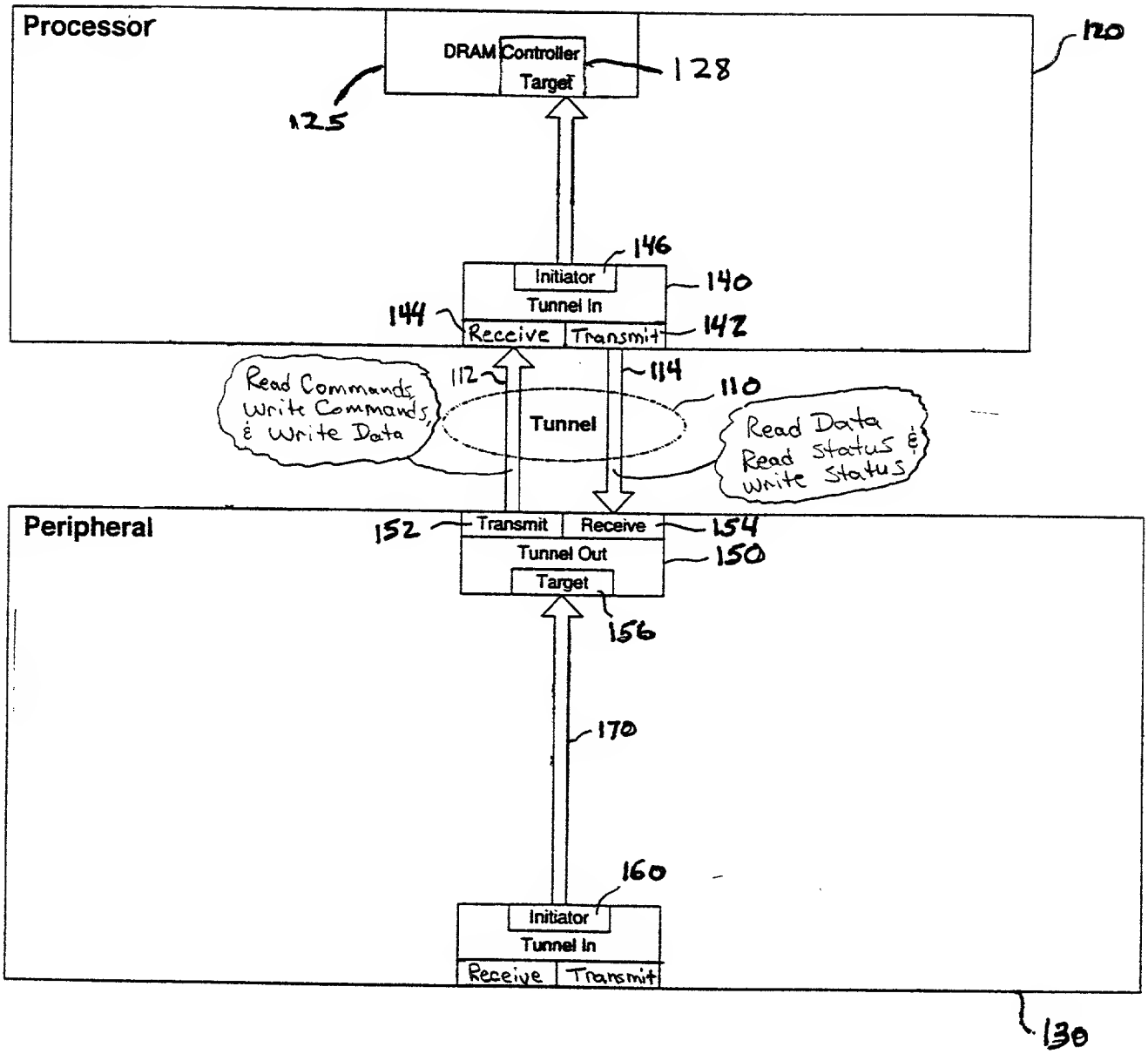

Processor
DRAM Controller
Target
128
125
120
146
Initiator
140
Tunnel In
144
Receive
Transmit
142
112
114
110
Tunnel
Read Commands, Write Commands, & Write Data
Read Data, Read Status, & Write Status
Peripheral
152
Transmit
Receive
154
Tunnel Out
150
Target
156
170
160
Initiator
Tunnel In
Receive
Transmit
130

FIG. 1

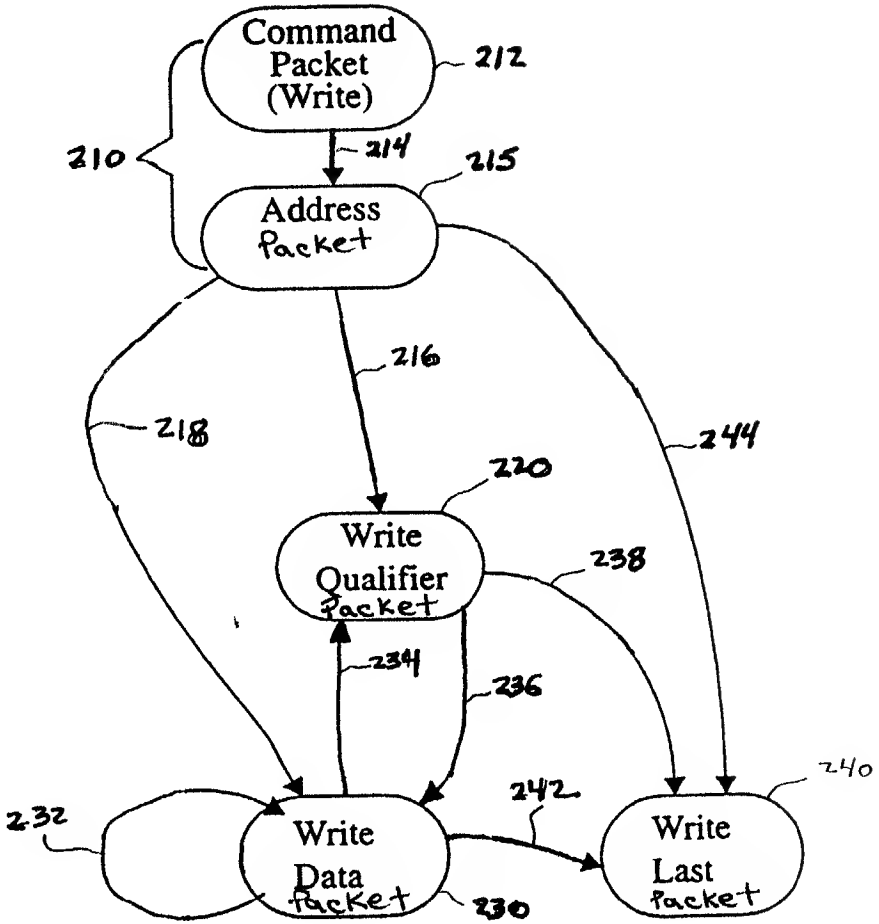


FIG. 2A

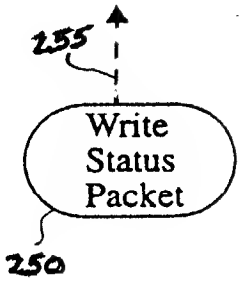


FIG. 2B

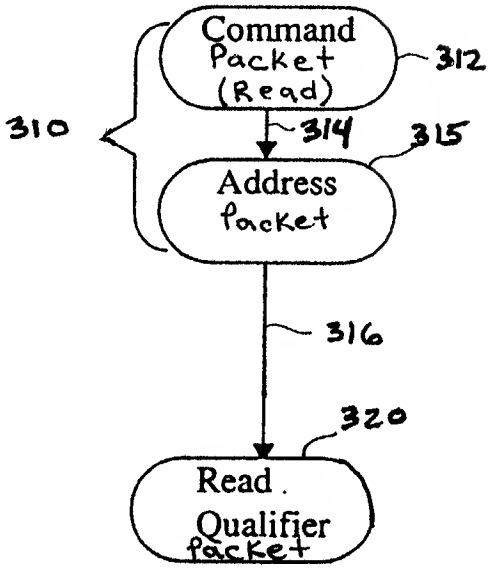


FIG. 3A

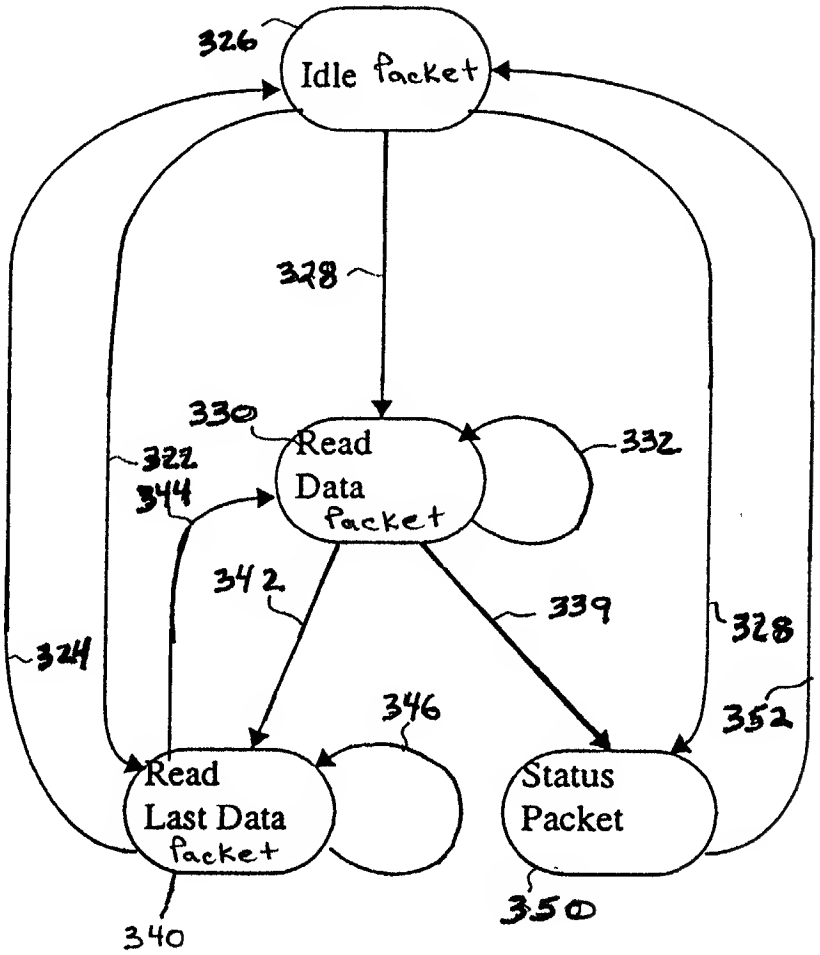
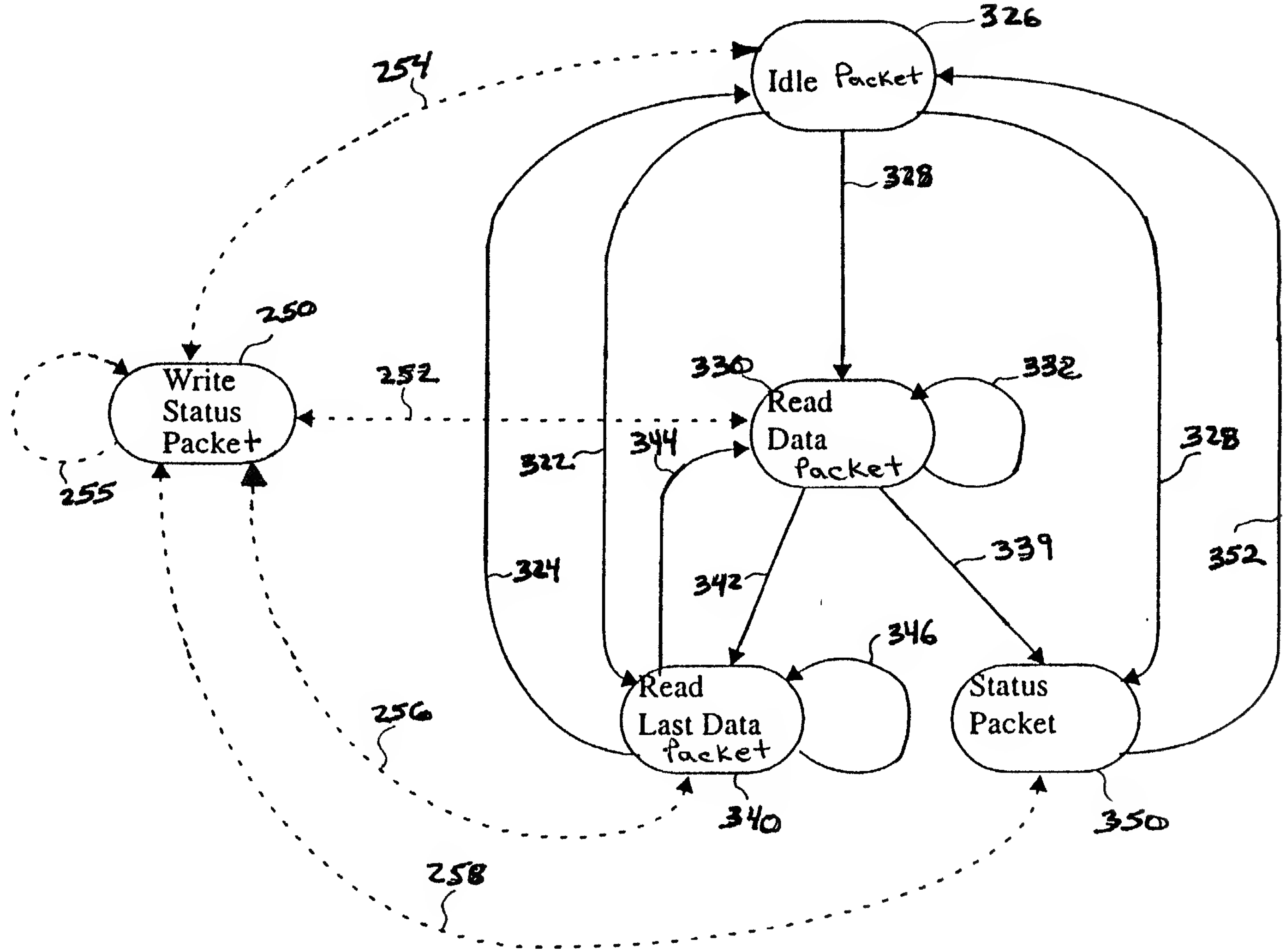
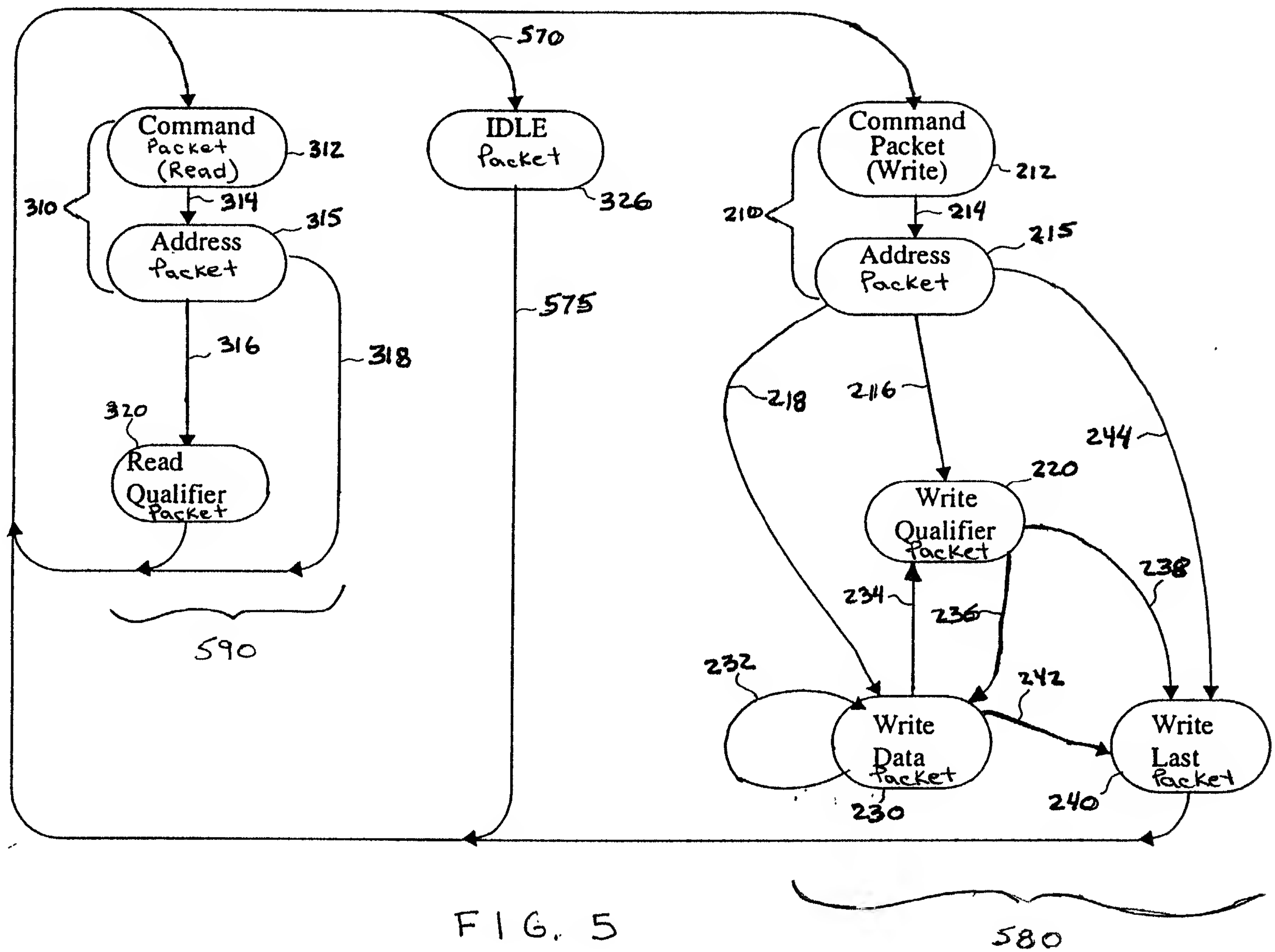


FIG. 3B



Idle Packet
326
328
Write
Status
Packet
250
252
255
254
Read
Data
Packet
330
332
322
344
328
324
342
339
352
346
Read
Last Data
Packet
Status
Packet
256
340
350
258

FIG. 4


Command Packet (Read)
312
314
310
Address Packet
315
316
318
320
Read Qualifier Packet
590
570
IDLE Packet
326
575
Command Packet (Write)
212
214
210
Address Packet
215
216
218
244
220
Write Qualifier Packet
238
234
236
232
242
Write Data Packet
230
Write Last Packet
240
580

F I G. 5

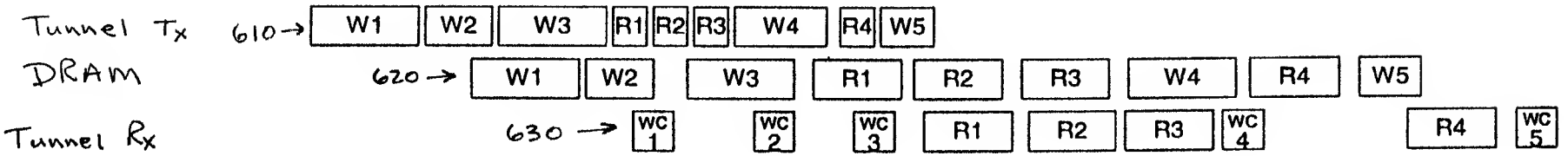


FIG. 6A

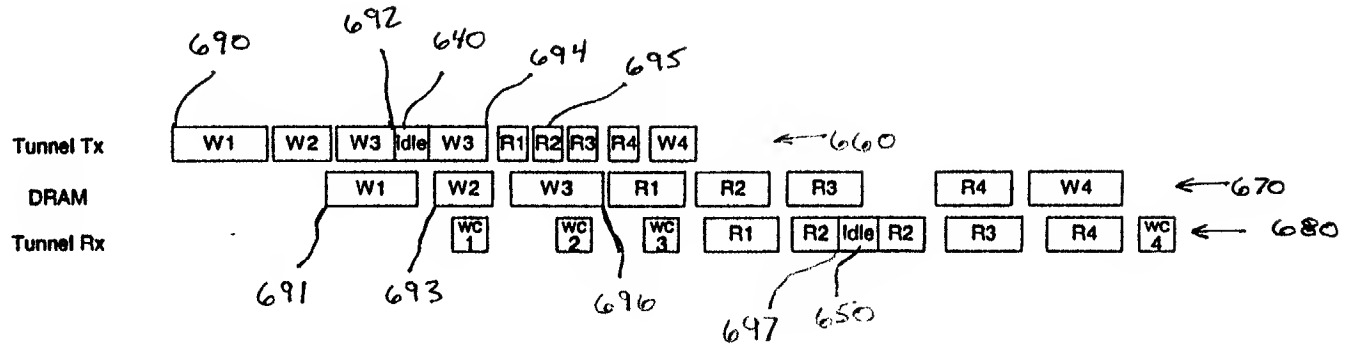


FIG. 6B